

**Remarks**

In the Office Action dated March 8, 2005, the Examiner rejected claims 1-4, 6 and 7 as unpatentable over Li et al. (US 6,309,933) in view of Yagashita et al. (US 6,607,952) and rejected claim 5 as unpatentable over Li et al. and Yagashita et al., and further in view of Bovaird (U.S. 4,830,975). In light of the forgoing amendments and the following remarks, the applicant respectfully submits that all rejections are traversed and claims 1-7 are in condition for allowance.

As an initial matter, claims 1 and 7 have been amended to overcome all of the objections to informalities and the rejections under 35 USC § 112.

Turning to the rejection of claims 1-7 as unpatentable over Li et al. in view of Yagashita et al., claim 1 recites, *inter alia*, a method for manufacturing a MOSFET device, including forming a low doped drain in the active region before forming the gate (part (b) in claim 1).

Li et al. disclose a method of fabricating a semiconductor transistor device including forming a pad dielectric layer over an upper silicon layer (column 3, lines 33-35) and a well implant within a well region in the upper silicon layer (column 2 lines 41-47). According to Li et al., after a gate is formed, LDD implants may be formed by an angled LDD ion implantation (column 5, lines 56-57). Although Li et al. disclose that ions are implanted in the substrate before forming the gate, the implantation does not form a low doped drain but, rather, forms a well. In Li et al., the low doped drain is formed after forming the gate. Accordingly, an implantation for forming the low doped drain requires an angled implantation (column 5, lines 56-57). Li et al. does not teach or suggest that the LDD may be formed prior to the formation of the gate.

Yagashita et al. disclose a method of manufacturing a semiconductor device. The semiconductor device of Yagashita et al. has a trench formed in an element isolation region surface of the substrate. A silicon oxide film is buried in the trench, thereby forming the element isolation insulating film having a shallow trench isolation structure (column 5, lines 29-38). However, Yagashita et al. do not disclose or suggest implanting ions in a first oxide layer to form a low doped drain prior to forming a gate.

Bovaird is directed to a method of manufacturing a planar recessed isolated MOS device. Bovaird does not disclose or suggest implanting ions in a first oxide layer to form a low doped drain prior to forming a gate.

It is respectfully submitted that none of the cited references referred to above discloses or suggests forming a LDD implantation prior to the formation of the gate. Therefore, none of the references can anticipate or make obvious the methods recited in the claims. Thus, it is respectfully submitted that all objections to the claims have been traversed and that the independent claim 1 and claims 2-7 dependent thereon are now in condition for allowance.

Reconsideration of the application and allowance thereof are respectfully requested. If there is any matter that the examiner would like to discuss, the examiner is invited to contact the undersigned representative at the telephone number set forth below.

Respectfully submitted,

Hanley, Flight & Zimmerman, LLC  
20 North Wacker Drive  
Suite 4220  
Chicago, Illinois 60606

Dated: June 27, 2005

A handwritten signature in black ink, appearing to read 'M.C. Zimmerman', is written over a horizontal line.

Mark C. Zimmerman  
Registration No. 44,006  
Attorney for Applicant  
(312) 580-1020